CLAIMS

1. A semiconductor memory device including a plurality of selecting lines for writing or reading data by selecting a specific memory cell from among a plurality of memory cells on the basis of the address signal supplied from external, comprising:

at least one first redundancy selecting line positioned at one of the ends in a plurality of said selecting lines and at least one second redundancy selecting line positioned at the other end; and

a switch circuit for changeably connecting a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and said redundancy selecting lines;

wherein, when any fault occurs in a plurality of said selecting lines, a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line is executed, or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line is executed, or both of said first and second switch operations are executed.

2. A semiconductor memory device according to claim 1, wherein, when the faults occur in two of a plurality of said selecting lines, both of said first and second switch operations are executed.

3. A semiconductor memory device according to claim 2, wherein, when a plurality of said selecting lines are disposed in alignment in the transverse direction and when the faults occur in two of said selecting lines, said first switch operation is executed by shifting at least one of said decode signal lines in the left direction and said second switch operation is executed by shifting at least one of said decode signal lines in the right direction.

4. A semiconductor memory device according to

claim 1, wherein, when a fault occurs in one of a plurality of said selecting lines, either one of said first and second switch operations is executed.

5. A semiconductor memory device according to claim 4, wherein, when a plurality of said selecting lines are disposed in alignment in the transverse direction and when a fault occurs in one of said selecting lines, said first switch operation is executed by shifting at least one of said decode signal lines in the left direction, or said second switch operation is executed by shifting at least one of said decode signal lines in the right direction.

6. A semiconductor memory device including a plurality of selecting lines for writing or reading data by selecting a specific memory cell from among a plurality of memory cells on the basis of an address signal supplied from external, comprising:

at least one first redundancy selecting line positioned at one of the ends among a plurality of said selecting lines and at least one second redundancy selecting line positioned at the other end;

a switch unit including a plurality of switch devices for changeably connecting a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

a shift redundancy fuse circuit unit having a plurality of fuses disposed so as to correspond to a plurality of said selecting lines and to said redundancy selecting lines, and cutting said fuses corresponding to fault selecting lines when faults occur in a plurality of said selecting lines, and fuses for redundancy selection, corresponding to said redundancy selecting lines; and

a shift redundancy control circuit unit for controlling a plurality of said switch devices in such a manner as to execute a first switch operation for

shifting at least one of said decode signal lines in the direction of said first redundancy selecting line, or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second operations, in accordance with the output result from said shift redundancy fuse circuit unit.

7. A semiconductor memory device according to claim 6, wherein, when faults occur in two of a plurality of said selecting lines, said shift redundancy fuse circuit unit cuts said fuses corresponding to two fault selecting lines in which the faults occur and said redundancy selecting fuses corresponding to said redundancy selecting line, and said shift redundancy control circuit unit controls a plurality of said switch devices in such a manner as to execute both of said first and second switch operations.

8. A semiconductor memory device according to claim 7, wherein, when a plurality of said selecting lines are disposed in alignment in the transverse direction and when faults occur in two of said selecting lines, said first switch operation is executed by shifting at least one of said decode signal lines in the left direction and said second switch operation is executed by shifting at least one of said decode signal lines in the right direction.

9. A semiconductor memory device according to claim 7, wherein the output result from said shift redundancy fuse circuit unit is outputted by a level of a DC voltage representing whether or not said fuses corresponding to said fault selecting lines and said redundancy selecting fuses are cut.

10. A semiconductor memory device according to claim 7, wherein said shift redundancy control circuit unit includes a NAND gate for outputting a shift control signal for shifting a plurality of said selecting lines in either direction upon receiving the output result from

said shift redundancy fuse circuit unit, and an inverter for inverting said shift control signal from said NAND gate.

11. A semiconductor memory device according to claim 7, wherein said shift redundancy control circuit unit includes a NOR gate for outputting a shift control signal for shifting a plurality of said selecting lines in either direction upon receiving the output result from said shift redundancy fuse circuit unit, and an inverter for inverting said shift control signal from said NOR gate.

12. A semiconductor memory device according to claim 7, wherein each of a plurality of said switch devices inside said switch unit is a three-directional switch device capable of selecting a mode for executing the shift operation in the direction of said first redundancy selecting line, a mode for executing the shift operation in the direction of said second redundancy selecting line or a mode for not executing said shift operations.

13. A semiconductor memory device according to claim 12, wherein each of a plurality of said switch devices can select a non-selection mode for not connecting said decode signal line to said fault selecting line.

14. A semiconductor memory device according to claim 7, wherein said shift redundancy fuse circuit unit includes a fuse circuit for normal selection that is used for a normal operation, a fuse circuit for redundancy selection that is used for redundancy selection, and a fuse circuit for forced redundancy that is used for forced redundancy.

15. A semiconductor memory device according to claim 7, wherein said shift redundancy fuse circuit unit includes a fuse circuit for forced redundancy for causing a fuse corresponding to a predetermined selecting line to look as being apparently cut at the time of forced

redundancy in order to confirm whether or not any fault exists in said redundancy selecting lines.

16. A semiconductor memory device according to claim 15, wherein said selecting line connected to said fuse circuit for forced redundancy is disposed at a position other than the adjacent position of said redundancy selecting line.

17. A semiconductor memory device according to claim 6, wherein, when any fault occurs in one of a plurality of said selecting lines, said shift redundancy fuse circuit unit cuts the fuse corresponding to said fault selecting line in which said fault occurs and said redundancy selecting fuse corresponding to said redundancy selecting line, and said shift redundancy control circuit unit controls a plurality of said switch devices in such a manner as to execute either one of said first and second switch operations.

18. A semiconductor memory device according to claim 17, wherein, when a plurality of said selecting lines are disposed in alignment in the transverse direction and when a fault occurs in one of a plurality of said selecting lines, said first switch operation is executed by shifting at least one of said decode signal lines in the left direction or said second switch operation is executed by shifting at least one of said decode signal lines in the right direction.

19. A semiconductor memory device according to claim 17, wherein the output result from said shift redundancy fuse circuit unit is outputted by a level of DC voltage representing whether or not said fuse corresponding to said fault selecting line and said redundancy selecting fuse are cut.

20. A semiconductor memory device according to claim 17, wherein said shift redundancy control circuit unit includes a NAND gate for outputting a shift control signal for shifting a plurality of said selecting lines in either direction upon receiving the output result from

said shift redundancy fuse circuit unit, and an inverter for inverting said shift control signal from said NAND gate.

21. A semiconductor memory device according to claim 17, wherein said shift redundancy control circuit unit includes a NOR gate for outputting a shift control signal for shifting a plurality of said selecting lines in either direction upon receiving the output result from said shift redundancy fuse circuit unit, and an inverter for inverting said shift control signal from said NOR gate.

22. A semiconductor memory device according to claim 17, wherein each of a plurality of said switch devices inside said switch unit is a three-directional switch device capable of selecting a mode for executing a shift operation in one of the directions of said redundancy selecting lines, a mode for executing said shift operation in the other direction of said redundancy selecting lines, and a mode for not executing said shift operations.

23. A semiconductor memory device according to claim 22, wherein each of a plurality of said switch devices can select a non-selection mode in which said decode signal lines and said fault selecting lines are not connected.

24. A semiconductor memory device according to claim 17, wherein said shift redundancy fuse circuit unit includes a fuse circuit for normal selection that is used for normal selection, a fuse circuit for redundancy selection that is used for redundancy selection and a fuse circuit for forced redundancy that is used for forced redundancy.

25. A semiconductor memory device according to claim 17, wherein said shift redundancy fuse circuit unit includes a fuse circuit for forced redundancy for causing a fuse corresponding to a predetermined selecting line to look as being apparently cut at the time of forced

redundancy, and confirms whether or not any fault exists in said redundancy selecting line.

26. A semiconductor memory device according to claim 25, wherein said selecting line connected to said fuse circuit for forced redundancy is disposed at a position other than the adjacent position to said redundancy selecting lines.

27. A semiconductor memory device according to claim 6, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

28. A semiconductor memory device according to claim 6, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

29. A semiconductor memory device according to claim 6, wherein a plurality of said selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

30. A semiconductor memory device according to claim 7, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

31. A semiconductor memory device according to claim 7, wherein the data write or read operation is executed in such a manner that that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

32. A semiconductor memory device according to claim 7, wherein a plurality of said selecting lines and a plurality of said fuses are laid out in the same pitch

in the semiconductor chip.

33. A semiconductor memory device according to claim 8, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

34. A semiconductor memory device according to claim 8, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cells selected by said selecting lines.

35. A semiconductor memory device according to claim 8, wherein a plurality of said selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

36. A semiconductor memory device according to claim 9, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one fuse is cut in the block of a plurality of said memory cells.

37. A semiconductor memory device according to claim 9, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

38. A semiconductor memory device according to claim 9, wherein a plurality of said selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

39. A semiconductor memory device according to claim 10, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one fuse is cut in the block of a plurality of said memory cells.

40. A semiconductor memory device according to claim 10, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

41. A semiconductor memory device according to claim 10, wherein a plurality of selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

42. A semiconductor memory device according to claim 11, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of memory cells.

43. A semiconductor memory device according to claim 11, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

44. A semiconductor memory device according to claim 11, wherein a plurality of said selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

45. A semiconductor memory device according to claim 12, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

46. A semiconductor memory device according to claim 12, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

47. A semiconductor memory device according to claim 12, wherein a plurality of said selecting lines and

a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

48. A semiconductor memory device according to claim 13, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

49. A semiconductor memory device according to claim 13, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

50. A semiconductor memory device according to claim 13, wherein a plurality of said selecting lines and a plurality of fuses are laid out in the same pitch in the semiconductor chip.

51. A semiconductor memory device according to claim 14, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

52. A semiconductor memory device according to claim 14, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

53. A semiconductor memory device according to claim 14, wherein a plurality of selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

54. A semiconductor memory device according to claim 15, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the

block of a plurality of memory cells.

55. A semiconductor memory device according to claim 15, wherein the data write or read operation is executed in such a manner that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

56. A semiconductor memory device according to claim 15, wherein a plurality of said selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

57. A semiconductor memory device according to claim 16, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

58. A semiconductor memory device according to claim 16, wherein periodicity of a plurality of memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

59. A semiconductor memory device according to claim 16, wherein a plurality of said selecting lines and a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

60. A semiconductor memory device according to claim 17, which detects whether or not said redundancy selecting lines are used by evaluating the output level of said shift redundancy fuse circuit unit and judging whether or not at least one of said fuses is cut in the block of a plurality of said memory cells.

61. A semiconductor memory device according to claim 17, wherein the data write or read operation is executed so that periodicity of a plurality of said memory cells is in conformity with periodicity of said memory cell block selected by said selecting lines.

62. A semiconductor memory device according to claim 17, wherein a plurality of said selecting lines and

a plurality of said fuses are laid out in the same pitch in the semiconductor chip.

63. A semiconductor memory device including a plurality of selecting lines for writing or reading data by selecting a specific memory cell from among a plurality of memory cells on the basis of the address signal supplied from external, comprising:

at least one first redundancy selecting line positioned at one of the ends among a plurality of said selecting line and at least one second redundancy selecting line positioned at the other end;

a switch unit including a plurality of switch devices for changeably connecting a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

a fuse decoder circuit for designating the address of said fuse corresponding to a fault selecting line, in which a fault occurs, when the fault occurs in a plurality of said selecting lines, and generating a fuse decode signal; and

a shift redundancy control circuit unit for controlling a plurality of said switch devices in such a manner as to execute a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second switch operations in accordance with a fuse decode signal from said fuse decode circuit.

64. A semiconductor memory device according to claim 63, wherein, when faults occur in two of a plurality of said selecting lines, said fuse decode circuit designates the addresses of said fuses corresponding to said two fault selecting lines in which the faults occur, and generates said fuse decode signal,

and said shift redundancy control circuit unit controls a plurality of said switch devices in such a manner as to execute both of said first and second switch operations.

65. A semiconductor memory device according to claim 64, wherein designation of the address of said fuse corresponding to each of said fault selecting lines by said fuse decoder circuit is made by the combination of a smaller number of a plurality of said fuses than the total number of a plurality of said selecting lines.

66. A semiconductor memory device according to claim 64, wherein said fuse decoder circuit includes two fuse decoder units for decoding signals generated by the combinations of a plurality of said fuses that are mutually different.

67. A semiconductor memory device according to claim 63, wherein, when a fault occurs in one of a plurality of said selecting lines, said fuse decoder circuit designates the address of said fuse corresponding to said fault selecting line in which the fault occurs, and generates a fuse decode signal, and said shift redundancy control circuit unit controls a plurality of said switch devices in such a manner as to execute either one of said first and second switch operations.

68. A semiconductor memory device according to claim 67, wherein designation of the address of said fuse corresponding to said fault selecting line by said fuse decoder circuit is made by a smaller number of a plurality of said fuses than the total number of a plurality of said selecting lines.

69. A semiconductor memory device according to claim 67, wherein said fuse decoder circuit includes two fuse decoder units for decoding signals generated by the combinations of a plurality of said fuses that are mutually different.

70. A semiconductor memory device including a plurality of selecting lines for writing or reading data by selecting a specific memory cell, from among a

plurality of memory cells provided to each of a plurality of cell arrays on the basis of the address signal supplied from external, including, for each of a plurality of said cell arrays:

at least one first redundancy selecting line positioned at one of the ends among a plurality of said selecting lines and at least one second redundancy selecting line positioned at the other end;

a switch unit including a plurality of switch devices for connecting changeably a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

a fuse decoder circuit for designating the address of said fuse corresponding to a fault selecting line, in which a fault occurs, and generating a fuse decode signal on the basis of the combination of a smaller number of a plurality of said fuses than the total number of a plurality of said selecting lines; and

a shift redundancy control circuit unit for controlling a plurality of said switch devices in such a manner as to execute a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at lest one of said decode signal lines in the direction of said second redundancy selecting lines or both of said first and second switch operations, in accordance with the fuse decode signal from said fuse decoder circuit;

wherein:

said shift redundancy fuse circuit unit having a plurality of said fuses is shared by said cell arrays adjacent to one another.

71. A semiconductor memory device according to claim 70, wherein said shift redundancy fuse circuit unit includes a fuse circuit for normal selection that is used for normal operation, a fuse circuit for redundancy

selection that is used for redundancy selection and a fuse circuit for forced redundancy that is used for forced redundancy.

72. A semiconductor memory device according to claim 70, wherein said fuse circuit for normal selection and said fuse circuit for forced redundancy are shared by said cell arrays adjacent to one another.

73. A semiconductor memory device according to claim 71, wherein said fuse circuits for redundancy selection are independently provided to said adjacent cell arrays.

74. A semiconductor memory device according to claim 70, which can execute said first switch operation or said second switch operation or both of said first and second operations for a plurality of said selecting lines of either one of said adjacent cell arrays, or can execute said first switch operation or said second switch operation or both of said first and second switch operations for a plurality of said selecting lines of both of said adjacent cell arrays.

75. A semiconductor memory device according to claim 71, which can execute said first switch operation or said second switch operation or both of said first and second switch operations for a plurality of selecting lines of either one of said adjacent cell arrays, or can execute said first switch operation or said second switch operation or both of said first and second switch operations for a plurality of selecting lines of both of said adjacent cell arrays.

76. A semiconductor memory device according to claim 72, which can execute said first switch operation or said second switch operation or both of said first and second switch operations for a plurality of said selecting lines of either one of said adjacent cell arrays, or can execute said first switch operation or said second switch operation or both of said first and second switch operations for a plurality of said

selecting lines of both of said adjacent cell arrays.

77. A semiconductor memory device according to claim 73, which can execute said first switch operation or said second switch operation or both of said first and second switch operations for a plurality of said selecting lines of either one of said adjacent cell arrays, or can execute said first switch operation or said second switch operation or both of said first and second switch operations for a plurality of said selecting lines of both of said adjacent cell arrays.

78. A semiconductor memory device including a plurality of column selecting lines for writing or reading data by selecting a specific memory cell, from among a plurality of memory cells constituting each of a plurality of memory cell blocks on the basis of the address signal supplied from external, wherein each of said memory cell blocks is divided into a plurality of row blocks and each of said memory cell blocks comprises:

at least one first redundancy selecting line positioned at one of the ends in a plurality of said column selecting lines and at least one second redundancy selecting line positioned at the other end;

a switch unit including a plurality of switch devices for changeably connecting a plurality of decode signal lines decoding said address signal to a plurality of said column selecting lines and to said redundancy selecting lines;

a redundancy fuse circuit unit including a smaller number of a plurality of fuses than the total number of a plurality of said column selecting lines and a plurality of redundancy selecting fuses disposed so as to correspond to said redundancy selecting lines, respectively;

a fuse decoder circuit for designating the address of a fuse corresponding to a fault selecting line in which a fault occurs, when said fault occurs in a plurality of said column selecting lines, and generating

a fuse decode signal on the basis of the combination of a plurality of said fuses; and

a shift redundancy control circuit unit for controlling a plurality of switch devices in such a manner as to execute a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second operations in accordance with said fuse decode signal from said fuse decoder circuit; and

wherein:

said first switch operation, or said second switch operation, or both of said first and second switch operations, are executed, or both of said first and second switch operations are not executed, for each of a plurality of said row blocks, on the basis of the logical addresses of a plurality of said row blocks.

79. A semiconductor memory device according to claim 78, wherein said fuse decode signal from said fuse decoder circuit is generated on the basis of said logical address.

80. A semiconductor memory device according to claim 78, wherein said shift redundancy fuse circuit unit includes a fuse circuit for normal selection that is used for a normal operation, a fuse circuit for redundancy selection that is used for redundancy selection and a fuse circuit for forced redundancy that is used for forced redundancy.

81. A semiconductor memory device according to claim 79, wherein said shift redundancy fuse circuit unit includes a fuse circuit for normal selection that is used for a normal operation, a fuse circuit for redundancy selection that is used for redundancy selection and a fuse circuit for forced redundancy that is used for forced redundancy.

82. A semiconductor memory device including a plurality of column selecting lines for writing or reading data by selecting a specific memory cell, from among a plurality of memory cells constituting each of a plurality of memory cell blocks, on the basis of the address signal supplied from external, wherein each of a plurality of said memory cell blocks is divided into a plurality of row blocks, and each of a plurality of said memory cell blocks comprises:

at least one first redundancy selecting line positioned at one of the ends among a plurality of said column selecting lines and at least one second redundancy selecting line positioned at the other end;

a switch unit including a plurality of switch devices for changeably connecting a plurality of decode signal lines decoding said address signal to a plurality of said column selecting lines and to a plurality of said redundancy selecting lines;

a shift redundancy fuse circuit unit including a plurality of fuses disposed so as to correspond to a plurality of said column selecting lines and to said redundancy selecting lines, respectively, and cutting a fuse corresponding to a fault selecting line in which a fault occurs, when the fault occurs in a plurality of said column selecting lines, and a redundancy selecting fuse corresponding to said redundancy selecting line; and

a shift redundancy control circuit unit for controlling a plurality of said switch devices in such a manner as to execute a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signals in the direction of said second redundancy selecting line or both of said first and second switch operations, in accordance with the output result from said shift redundancy fuse circuit unit; and

wherein:

said first switch operation or said second switch operation or both of said first and second switch operations are executed, or both of said first and second switch operations are not executed, on the basis of the logical addresses of a plurality of said row blocks.

83. A semiconductor memory device according to claim 82, wherein the output result of said shift redundancy fuse circuit unit is generated on the basis of said logical address.

84. A semiconductor memory device according to claim 83, wherein said shift redundancy fuse circuit unit includes a fuse circuit for normal selection that is used for a normal operation, a fuse circuit for redundancy selection that is used for redundancy selection and a fuse circuit for forced redundancy that is used for forced redundancy.

85. A method for executing a shift redundancy operation comprising the steps of:

arranging a plurality of selecting lines for writing or reading data by selecting a specific memory cell from among a plurality of memory cells on the basis of the address signal supplied from external, using said selecting line positioned at one of the ends among a plurality of said selecting lines as at least one first redundancy selecting line and using said selecting line positioned at the other end as at least one second redundancy selecting line;

connecting changeably a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines; and

executing a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second

redundancy selecting line or both of said first and second switch operations, when faults occur in a plurality of said selecting lines.

86. A method for executing a shift redundancy operation according to claim 85, wherein both of said first and second switch operations are executed when the faults occur in two selecting lines among a plurality of said selecting lines.

87. A method for executing a shift redundancy operation according to claim 85, wherein either one of said first and second switch operations is executed when the fault occurs in one selecting line among a plurality of said selecting lines.

88. A method for executing a shift redundancy operation comprising the steps of:

arranging a plurality of selecting lines for writing or reading data by selecting a specific memory cell from among a plurality of memory cells on the basis of the address signal supplied from external, using a selecting line positioned at one of the ends among a plurality of said selecting lines as at least one first redundancy selecting line and using a selecting line positioned at the other end as at least one second redundancy selecting line;

connecting changeably a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

cutting a fuse corresponding to a fault selecting line in which a fault occurs, when the fault occurs in a plurality of selecting lines, and redundancy selecting fuses corresponding to said redundancy selecting lines, in a shift redundancy fuse circuit unit having a plurality of fuses; and

executing a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a

second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second switch operations, in accordance with the output result from said shift redundancy fuse circuit unit.

89. A method for executing a shift redundancy operation comprising the steps of:

arranging a plurality of selecting lines for writing or reading data by selecting a specific memory cell from among a plurality of memory cells on the basis of the address signal supplied from external, using a selecting line positioned at one of the ends among a plurality of said selecting lines as at least one first redundancy selecting line and using a selecting line positioned at the other end as at least one second redundancy selecting line;

connecting changeably a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

designating the address of a fuse corresponding to a fault selecting line in which a fault occurs and generating a fuse decode signal when the fault occurs in a plurality of said selecting lines; and

executing a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second switch operations, in accordance with said fuse decode signal.

90. A method for executing a shift redundancy operation comprising the steps of:

arranging a plurality of selecting lines for writing or reading data by selecting a specific memory cell, from among a plurality of memory cells

provided to each of a plurality of cell arrays on the basis of the address signal from external, using a selecting line positioned at one of the ends among a plurality of said selecting lines as at least one first redundancy selecting line and using a selecting line positioned at the other end as at least one second redundancy selecting line;

connecting changeably a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

causing said cell arrays adjacent to one another to share a shift redundancy circuit unit having a plurality of fuses;

designating the address of a fuse corresponding to a fault selecting line in which a fault occurs and generating a fuse decode signal when the fault occurs in a plurality of said selecting lines; and

executing a first switch operation for shifting at least one of said decode signal lines in the direction or said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second switch operations in accordance with said fuse decode signal from said fuse decoder circuit.

91. A method for executing a shift redundancy operation comprising the steps of:

arranging a plurality of column selecting lines for writing or reading data by selecting a specific memory cell, from among a plurality of memory cells constituting each of a plurality of memory cell blocks on the basis of the address signal supplied from external, each of said memory cell blocks being divided into a plurality of row blocks, using a column selecting line positioned at one of the ends among a plurality of said column selecting lines as at least one first redundancy

selecting line and using a column selecting line positioned at the other end as at least one second redundancy selecting line;

connecting changeably a plurality of decode signal lines decoding said address signal to a plurality of said column selecting lines and to said redundancy selecting lines;

designating the address of a fuse corresponding to a fault selecting line in which a fault occurs, and generating a fuse decode signal on the basis of the combination of a plurality of fuses in a shift redundancy fuse circuit unit having a plurality of said fuses when any fault occurs in a plurality of said column selecting lines; and

executing a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second switch operations or none of said first and second switch operations, independently for each of a plurality of said row blocks on the basis of the logical addresses of a plurality of said row blocks.

92. A method for executing a shift redundancy operation comprising the steps of:

arranging a plurality of column selecting lines for writing or reading data by selecting a specific memory cell, from among a plurality of memory cells constituting each of a plurality of memory cell blocks on the basis of the address signal supplied from external, each of said memory cell blocks being divided into a plurality of row blocks, using a column selecting line positioned at one of the ends among a plurality of column selecting lines as at least one first redundancy selecting line and using a column selecting line positioned at the other end as at least one second

redundancy selecting lines;

connecting changeably a plurality of decode signal lines decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

cutting a fuse corresponding to a fault selecting line in which a fault occurs and a redundancy selecting fuse corresponding to said redundancy selecting lines in a shift redundancy fuse circuit unit having a plurality of said fuses when any fault occurs in a plurality of said column selecting lines; and

executing a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting line or both of said first and second switch operations or none of said first and second switch operations, independently for each of a plurality of row blocks on the basis of the logical addresses of a plurality of said row blocks.

93. A semiconductor memory device including a plurality of selecting lines for writing or reading data by selecting a specific memory cell from among a plurality of memory cells on the basis of the address signal supplied from external, comprising:

at least two first redundancy selecting lines positioned at one of the ends among a plurality of selecting lines and at least two second redundancy selecting lines positioned at the other end; and

a first switch unit and a second switch unit disposed in at least two stages, for changeably connecting a plurality of decode signals decoding said address signal to a plurality of said selecting lines and to said redundancy selecting lines;

wherein:

when any fault occurs in a plurality of

said selecting lines, said first switch unit executes a first switch operation for shifting at least one of said decode signal lines in the direction of said first redundancy selecting line or a second switch operation for shifting at least one of said decode signal lines in the direction of said second redundancy selecting lines or both of said first and second switch operations; and

said second switch unit executes a third switch operation for shifting further at least one of said decode signals after said first switch operation in the direction of said first redundancy selecting line or a fourth switch operation for shifting further at least one of said decode signal lines after said second switch operation in the direction of said second redundancy selecting lines or both of said third and fourth switch operations or none of said third and fourth switch operations.

94. A semiconductor memory device according to claim 93, wherein, when faults occur in four of a plurality of said selecting lines, said first switch unit executes both of said first and second switch operations and said second switch unit executes both of said third and fourth switch operations.

95. A semiconductor memory device according to claim 93, wherein, when faults occur in three of a plurality of said selecting lines, said first switch unit executes both of said first and second switch operations and said second switch unit executes either one of said third and fourth switch operations.

96. A semiconductor memory device according to claim 93, wherein, when faults occur in two of a plurality of said selecting lines, said first switch unit executes either one of said first and second switch operations and said second switch unit executes either one of said third and fourth switch operations.

97. A semiconductor memory device according to claim 93, wherein, when faults occur in two of a

plurality of said selecting lines, said first switch unit executes both of said first and second switch operations and said second switch unit executes none of said third and fourth switch operations.

98. A semiconductor memory device according to claim 93, wherein, when a fault occurs in one of a plurality of said selecting lines, said first switch unit executes either one of said first and second switch operations and said second switch unit executes none of said third and fourth switch operations.